Docket No.: X2007.0148
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Yasunori Mizoguchi et al.

Application No.: 10/757,574

Confirmation No.: 4541

Filed: January 15, 2004

Art Unit: 2829

For: INSPECTION APPARATUS FOR PRINTED BOARD

Examiner: Chan, Emily Y.

SUBMISSION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to Applicants' Request for Continued Examination and the Information Disclosure Statement filed June 22, 2006, Applicants submit herewith an English translation of the Abstract of the Korean publication 1999-54226 and an English Abstract of Japanese unexamined patent application number 2001-83214. This Japanese unexamined patent application corresponds to Japanese application H11-260677 (JP 260677/1999) which is claimed as a priority application in the Chinese application which resulted in publication CN 1288160A cited in the IDS.

Applicants again respectfully submit that they have complied with the requirements of 37 CFR 1.56 and MPEP §609.04(a) III and that the Office must consider these references. MPEP §609.04(a) III states that:

> "Where the information listed is not in the English language, but was cited in a search report or other action by a Foreign patent

> office in a counterpart foreign application, the requirement for concise explanation of relevance can be satisfied by submitting an English language version of the search report which indicates the degree of relevance found of the Foreign office."

Applicants have fully fulfilled their duty of disclosure with respect to the previous IDS by providing the Office with full translations of the office actions from the foreign patent office that cited the references. As explained to the Examiner, the provision of these foreign office actions that cited the references satisfies Applicants' duty of supplying a concise explanation of the relevance of the references.

Applicants are providing the attached translations merely for the convenience of and at the request of the Examiner.

As Applicants have complied with the requirements of 37 CFR 1.56 and MPEP §609.04(a) III it is respectfully requested that the Office consider the references cited in the previous IDS.

Dated: July 6, 2006

Respectfully submitted,

By /Michael J. Scheer/
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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-083214
(43)Date of publication of application : 30.03.2001

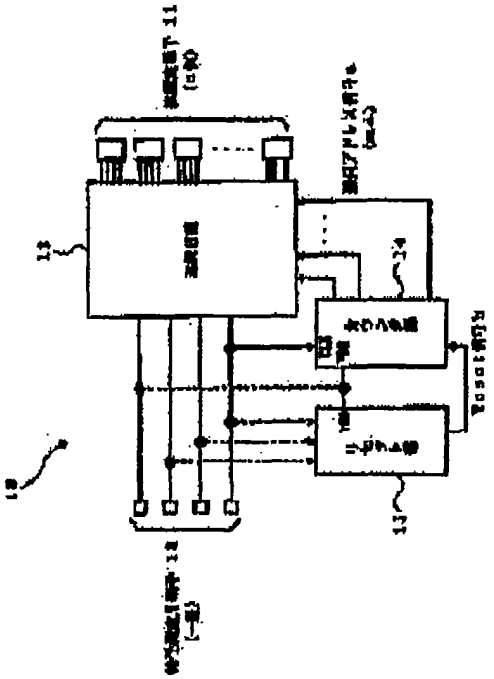
(51)Int.Cl. G01R 31/28

(21)Application number : 11-260677
(22)Date of filing : 14.09.1999

(71)Applicant : NEC CORP
(72)Inventor : OKAWA SHINICHI

(54) SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR ITS CHARACTERISTIC

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a semiconductor integrated circuit facilitating installation of a terminal at a periphery of a chip and needing no external controller for controlling generation of a selection address signal by limiting number of terminals for measuring characteristics to measure the characteristics of a plurality of elements to be measured.
SOLUTION: The semiconductor integrated circuit having a plurality of elements 11 to be measured and a terminal 13 for measuring characteristics comprises a counter 14 for outputting a selection address signal a for selectively connecting the plurality of the elements 11 to the terminal 13. In this case, the counter 14 is driven by a signal scanned when measured at the characteristics to automatically generate thee signal a.



LEGAL STATUS

[Date of request for examination]	08.08.2000
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	withdrawal
[Date of final disposal for application]	19.09.2001
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

English-language translation of the abstract attached to the Korean publication, 1999-54226.

Publication date: July 15, 1999
Applicant: Samsung Electronic Co. Ltd.
Title of the invention: Relay printed circuit board in test facilities

Abstract:

The present invention relates to test facilities, wherein a relay PCB is arranged in the test facilities; input/output pins at prescribed positions among a plurality of input/output pins formed in a single IC are only connected to the relay PCT and are then subjected to testing in a time-division manner, thus testing plenty of ICs at once; hence, it is possible to reduce the cost of testing and to improve the productivity.